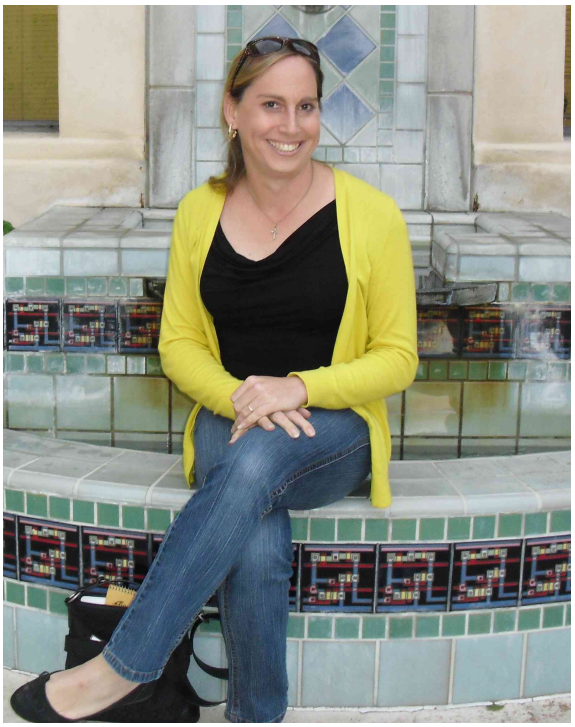
Integrated Computational Electronics Laboratory (ICE)



Is that layout on those tiles?

Welcome to the ICE Laboratory Site @ GT

The lab has two current focus directions:

- Programmable and configurable, analog and digital, circuits, signal processing, algorithms, and systems
- Neuromorphic Engineering

From these two areas of focus, we research signal processing, analog and digital integrated circuits and systems design, computational neuroscience, nonlinear dynamics, and CMOS device physics.

Lead Professor: Dr. Jennifer Hasler

Topically Organized Publications

Overview writings

Recent Courses Taught

Potential Senior Design / Graduate Special Problems directions

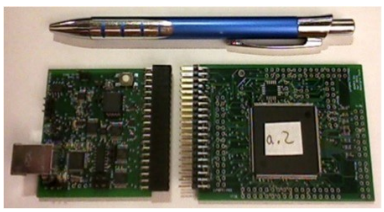
Recent article on the importance of the Faculty--Ph.D. Student Mentoring Relationship (GT press: April 11, 2016)

Some background on my former graduate students

Some of Dr. Hasler's personal thoughts (under construction)

"if you build it, you understand it. And if you understand it, you can build it" -- Carver Mead

Programmability and Configurability



Physical and Neuromorphic Computation

Neuromorphic Systems: have systems based on neuroscience, to perform biological like tasks, including robotics, and thereby contribute to neuroscience understanding.

- Large-Scale Field-Programmable Analog Array (FPAA) Overview in IEEE Proceedings [1].
- Short SoC FPAA Video Introduction by Sihwan Kim, Aishwarya Natarajan, and Sahil Shah
- Virtual Version of our FPAA workshops formed around the SoC FPAA
- FPAA design Scilab / Xcos tools [3]
- Download FPAA tools / Ubuntu VM
- First System on Chip (SoC) FPAA Integrated Circuit [2]
- Further SoC FPAA papers & resources
- Press articles on the SoC FPAA and infrastructure from Electronic Products [4] and GT press [5].
- Download FPAA Board Design Files

References :

[1] J. Hasler, "Large-Scale Field-Programmable Analog Arrays," *Proceedings of IEEE* , 2020.
[2] S. George, S. Kim, S. Shah, et. al, "A Programmable and Configurable Mixed-Mode FPAA SOC," *IEEE Transactions on VLSI*, 2016.
[3] M. Collins, J. Hasler, and S. George, "An Open-Source Toolset Enabling Analog–Digital–Software Codesign," *Journal of Low Power Electronics Applications*, January 2016.
[4] Electronic Product Magazine, March 21, 2016. "New analog chip uses 1,000 times less electrical power (and can be built a hundred times smaller) than comparable digital devices"
[5] http://www.rh.gatech.edu/news/508791 /configurable-analog-chip-computes-1000-times-less-power-digital

- Initial Physical Analog Computation Framework [1]. You can watch the presentation from ICRC 2016 conference at this link . This presentation was the first talk given at the first rebooting computing conference (ICRC).
- Further Physical Computing papers & resources
- IEEE Spectrum Roadmap Discussion [2], and Neuromorphic Roadmap paper [3].
- Further Neuromorphic papers & resources

References :

[1] J. Hasler, “Opportunities in Physical Computing driven by Analog Realization,” *IEEE IC Rebooting Computing* , San Deigo, October 2016.
[2] J. Hasler, "We could build an artificial brain right now," *IEEE Spectrum* , June 2017.
[3] J. Hasler, H. B. Marr, "Finding a Roadmap to achieve Large Neuromorphic Hardware Systems," Frontiers in Neuroscience, vol. 7, no. 118, September 2013. pp. 1-29. DOI=10.3389/fnins.2013.00118