SEARCH

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Scalable Array Packaging for Optoelectronic Components

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ABSTRACT

Array Packaging for Optoelectronic Components

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As part of the Engineering Research Center for Integrated Access Networks (CIAN), this project will investigate scalable and novel packaging for optoelectronic components, e.g. vertical cavity surface emitting laser (VCSEL) and tunable filter arrays. This will fill a major

need to enable research groups focusing on novel devices to bring forth components suitable for advanced characterization in systems and testbeds. The funding will support a research engineer with expertise and experience of industrial practice and innovation in optoelectronics and optical micro-electro-mechanical systems (MEMS). The particular candidate identified for this position is Dr. S. Patra, with 16 years of industry experience in process development and transfer. He will bring critical skill base to enhance Thrust III's capability to deliver advance proof-of-concept devices to test beds, and translate research ideas into system architecture.

In the optoelectronic components industry, the package cost accounts for 60 to 80% of current manufacturing expenses in component assembly, while it is only 10% in electronic components. To deploy the novel photonic and optoelectronic components proposed here in access networks in CIAN, one must address the packaging cost. The planned strategy is, first, to treat packaging as part of the device design rather than an afterthought; and, second, to pursue chip-scale packaging whenever possible. Chip-scale packaging is now widely employed in IC and MEMS industries to reduce footprint and packaging cost.

The project includes two major components of wafer-level, low-cost, hermetic packaging. The first one includes the process and package of a high-speed VCSEL array and the second with in-plane waveguide arrays. The challenge for the first project is the need of multiple chips requiring vertical alignments, while for the second is on requiring alignment of both facets of a chip. This covers the most challenging parts of fiber coupling problems: surface-emitting 2D array and coupling of both facets of edge-emitting devices. With solutions to both topologies, the developed results will be readily extended to all optoelectronic devices. Dr. Patra has significant industrial experiences on both types of packaging, particularly on thermal, mechanical and electric designs of optoelectronic packages. His leadership will help to prepare the graduate students to include packaging considerations into device and material designs and to work at the intersection. The key scientific goals and intellectual merit of this proposal is to develop a scalable process and bring forth a common platform to assemble diverse optoelectronic devices, requiring optical coupling in both surface-normal and in-plane directions, a range of electrical signal frequencies and operating conditions.

The broader impacts will be in effectively bridging the gap between optoelectronic devices and systems by providing a universal packaging platform. The proposed work will facilitate researchers to collaborate more readily within the Center and with industry. The new processes will be fundamental and can be readily extended to all edge-emitting and surface-emitting optoelectronic devices. This work will be important for low-cost, high through-put manufacturing of arrays of optoelectronic devices. The purpose of the CIAN Photonics Testbed is to be the first research facility to target cross-disciplinary research on communications systems spanning from fundamental devices to subsystems to systems. With the packaging know-how brought forth by Dr. Patra, the devices invented by Thrust 3 researchers will be able to participate more actively in the testbed. As CIAN sponsors REU students and high school outreach programs, this proposed work will provide better preparation for undergraduate and high school students with real world practices and research experiences.

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